module vending\_machine\_343(  input clk,input rst,input [1:0] in,output reg out);

parameter s0=2'b00;

parameter s1=2'b01;

parameter s2=2'b10;

reg [1:0]c\_state,n\_state;

always @(posedge clk)

begin

    if(rst==1)

    begin

        c\_state=0;

        n\_state=0;

    end

    else

    begin

    c\_state=n\_state;

    case(c\_state)

    s0: if(in==0)

    begin

        n\_state=s0;

        out=0;

    end

    else if(in==2'b01)

    begin

        n\_state=s1;

        out=0;

    end

    else if(in==2'b10)

    begin

    n\_state=s2;

    out=0;

    end

    s1: if(in==0)

    begin

        n\_state=s0;

        out=0;

    end

    else if(in==2'b01)

    begin

        n\_state=s2;

        out=0;

    end

    else if(in==2'b10)

    begin

    n\_state=s0;

    out=1;

    end

    s2: if(in==0)

    begin

        n\_state=s0;

        out=0;

    end

    else if(in==2'b01)

    begin

        n\_state=s0;

        out=1;

    end

    else if(in==2'b10)

    begin

    n\_state=s0;

    out=1;

    end

    endcase

    end

end

endmodule

TESTBENCH

`timescale 1ns/1ns

`include "vendingmachine.v"

module vending\_machine\_tb;

reg clk;

reg rst;

wire out;

reg [1:0] in;

vending\_machine\_343 uut(.clk(clk),.rst(rst),.in(in),.out(out));

always #5 clk=~clk;

initial begin

    $dumpfile("vendingmachine.vcd");

    $dumpvars(0,vending\_machine\_tb);

    rst=1;

    clk=0;

    #6 rst=0;

    in=1;

    #19 in=2;

    #100 $finish;

end

endmodule